IN THE CLAIMS

Please amend the claims as indicated below.

1. (currently amended) A field transistor containing no thin gate insulating layer comprising:

a well region of a first conductivity type;

a field oxide layer for defining an active region on the well region;

high concentration source and drain regions of a second conductivity type separated from each other by a width of the field oxide layer;

a low concentration source region of the second conductivity type formed in the well region, the low concentration source region being adjacent to the high concentration source region and overlapped by one end of the field oxide layer;

a low concentration drain region of the second conductivity type formed in the well region, the low concentration drain region being adjacent to the high concentration drain region and overlapped by the other end of the field oxide layer; and

a gate conductive layer pattern formed on the field oxide layer, the gate conductive layer pattern overlapping parts of the low concentration source and drain regions of the second conductivity type.

2. (original) The field transistor of claim 1, wherein the well region of the first conductivity type is formed on a high concentration buried region of the first conductivity type on a semiconductor substrate of the first conductivity type.

3. (previously amended) The field transistor of claim 1, wherein the well region of the first conductivity type is formed on a semiconductor substrate of the first conductivity type.

4. (original) The field transistor of claim 1, further comprising a high concentration diffusion region of the first conductivity type formed in the well region, the high concentration diffusion region being separated from the high concentration source region of the second conductive type by a predetermined distance.

5. (original) The field transistor of claim 4, further comprising a low concentration diffusion region of the first conductivity type and a low concentration diffusion region of the

second conductivity type, both low concentration diffusion regions being adjacent to each other between the high concentration diffusion region of the first conductivity type and the high concentration source region of the second conductivity type.

6. (original) The field transistor of claim 5, wherein the low concentration diffusion region of the first conductivity type is adjacent to the high concentration diffusion region of the first conductivity type, and the low concentration diffusion region of the second conductivity type is adjacent to the high concentration source region of the second conductivity type.

7. (original) The field transistor of claim 1, further comprising:

a gate electrode electrically connected to the gate conductive layer pattern;

a source electrode electrically connected to the high concentration source region of the second conductivity type; and

a drain electrode electrically connected to the high concentration drain region of the second conductivity type.

8. (original) The field transistor of claim 7, wherein the drain electrode is electrically connected to the gate electrode.

9. (original) The field transistor of claim 7, wherein the source electrode is electrically connected to the high concentration diffusion region of the first conductivity type as well.

10. (original) The field transistor of claim 1, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

11. through 18. (withdrawn)

19. (currently amended) A semiconductor device containing no thin gate insulating layer, comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over a portion of the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer; and

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region.

20. (original) The device of claim 19, further comprising a first diffusion region of the first conductivity type formed in the well region and separated from the first source region.

21. (original) The device of claim 20, further comprising a second diffusion region having a first conductivity type concentration lower than the first diffusion region and comprising a third diffusion region of the second conductivity type, both the second and third diffusion regions adjacent each other and located between the first diffusion region and the first source region.

22. (original) The device of claim 21, the second diffusion region type located adjacent the first diffusion region and the third diffusion region located adjacent the first source region.

23. (original) The device of claim 19, further comprising:

a gate electrode electrically connected to the conductive layer;

a source electrode electrically connected to the first source region; and

a drain electrode electrically connected to the first drain region.

24. (original) The device of claim 23, the drain electrode being electrically connected to the gate electrode.

25. (original) The device of claim 23, the source electrode being electrically connected to the first diffusion region.

26. (original) The device of claim 19, wherein the first conductivity type is p-type and the second conductivity type is n-type.

27. (currently amended) A semiconductor device containing no thin gate insulating layer, comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer;

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region;

a gate electrode electrically connected to the conductive layer;

a source electrode electrically connected to the first source region; and

a drain electrode electrically connected to the first drain region.

28. (original) The device of claim 27, further comprising a first diffusion region of the first conductivity type formed in the well region and separated from the first source region, a second diffusion region having a first conductivity type concentration lower than the first diffusion region, and a third diffusion region of the second conductivity type, wherein both the second and third diffusion regions are adjacent each other and located between the first diffusion region and the first source region.

29. (currently amended) A system for electrostatic discharge protection containing a field transistor without a thin gate insulating layer, the field transistor comprising:

a substrate comprising a well region of a first conductivity type;

a field oxide layer located over the well region;

a first source region of a second conductivity type and a first drain region of a second conductivity type separated by the field oxide layer;

a second source region having a second conductivity type concentration lower than the first source region, the second source region formed in the well region adjacent the first source region with a portion of the second source region underlying the field oxide layer;

a second drain region having a second conductivity type concentration lower than the first drain region, the second drain region formed in the well region adjacent the first drain region with a portion of the second drain region underlying the field oxide layer; and

a conductive layer formed over the field oxide layer, the conductive layer overlapping the second source region and the second drain region.

30. through 39. (withdrawn)

40. (original) A semiconductor device for electrostatic discharge protection, the device comprising a field transistor having both a source region and a drain region overlapped by a gate conductive layer while containing no gate insulating layer.

41. (original) A system for electrostatic discharge protection, the system comprising a field transistor having both a source region and a drain region overlapped by a gate conductive layer while containing no gate insulating layer.